T1 T2 T3 T4 T5 IF RD EXE MEM WB
IF RD
<u>L</u>
:
:

Fig. 1

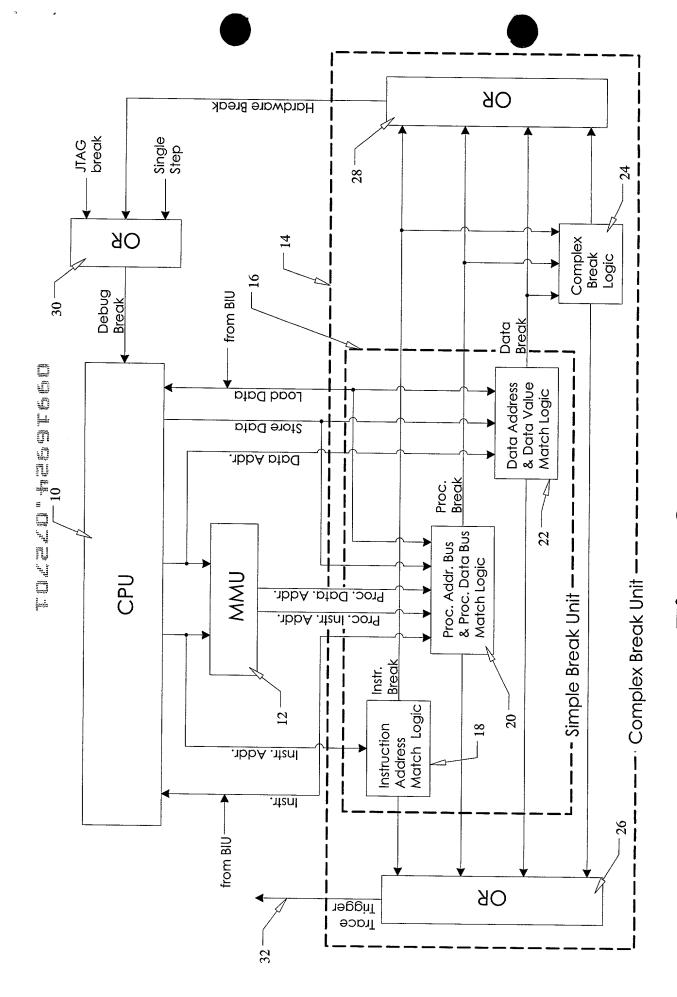


Fig. 2

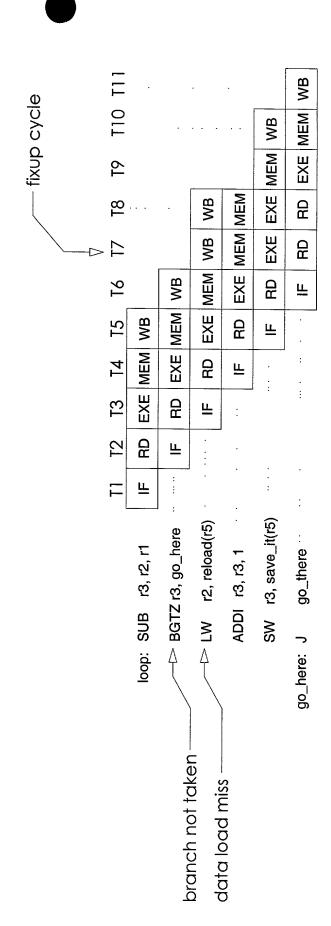


Fig. 3

